

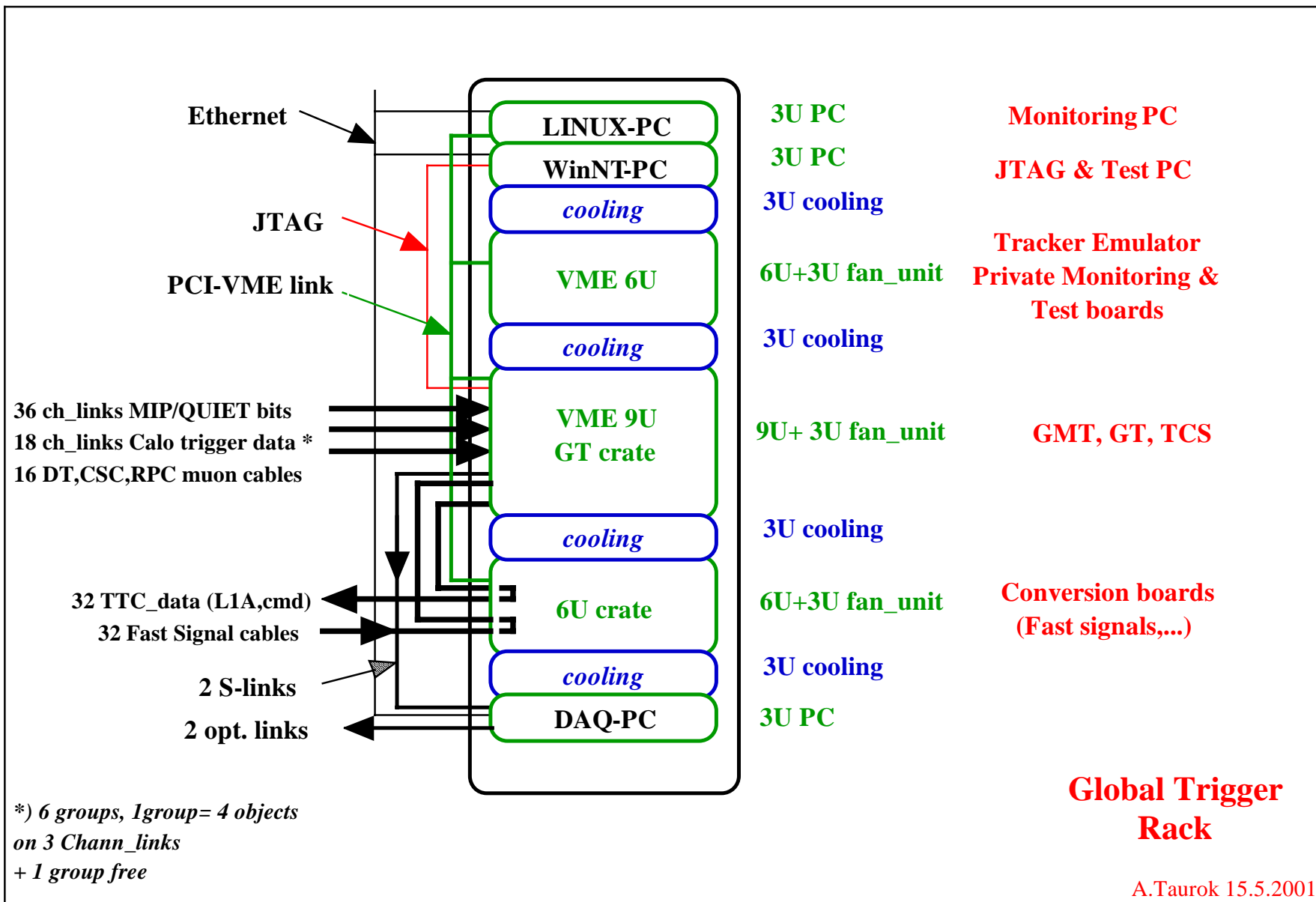
Status of
Global Trigger
Global Muon Trigger

Sept 2001

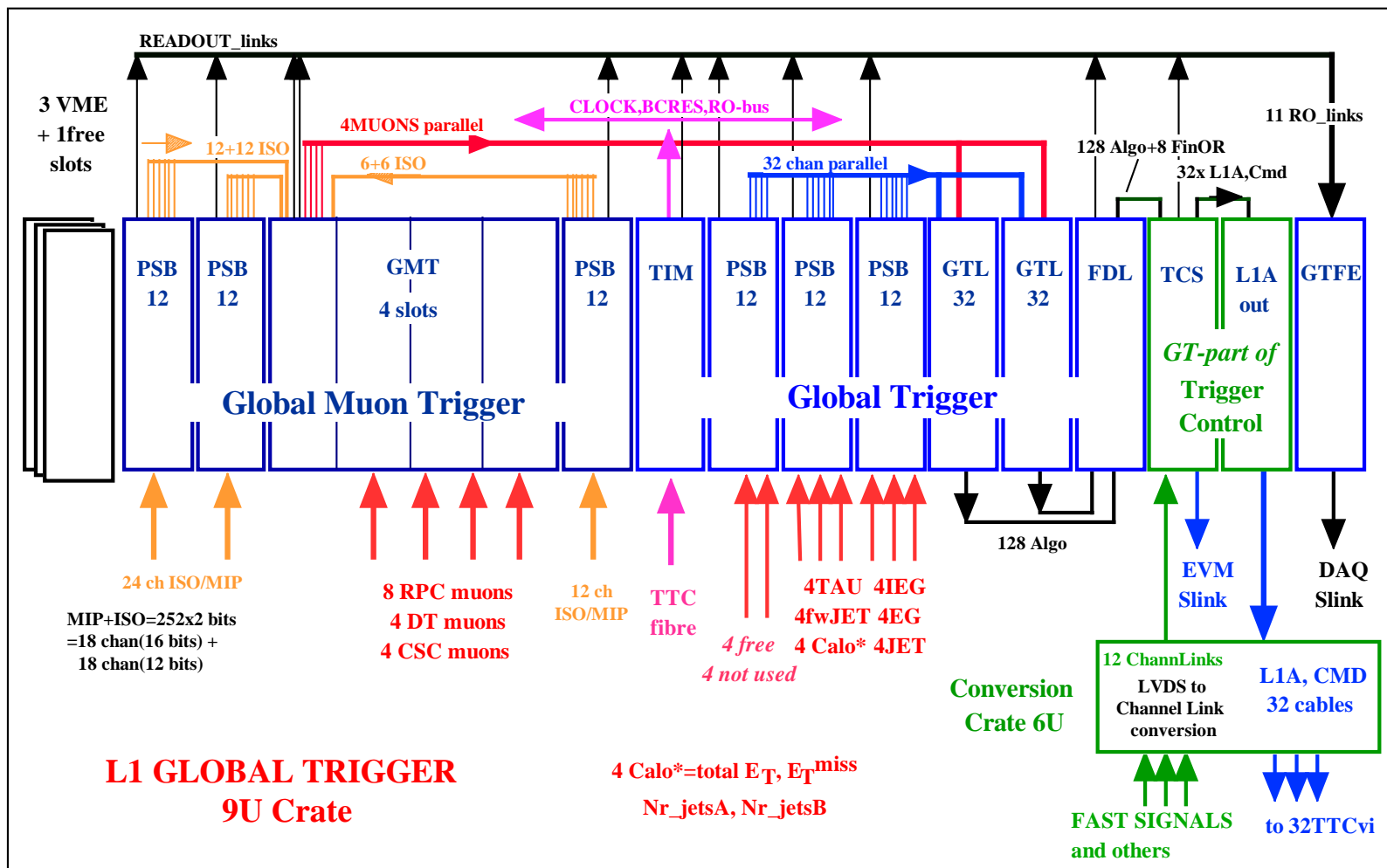
Vienna CMS-group

presented by A.Taurok

Global Trigger Rack

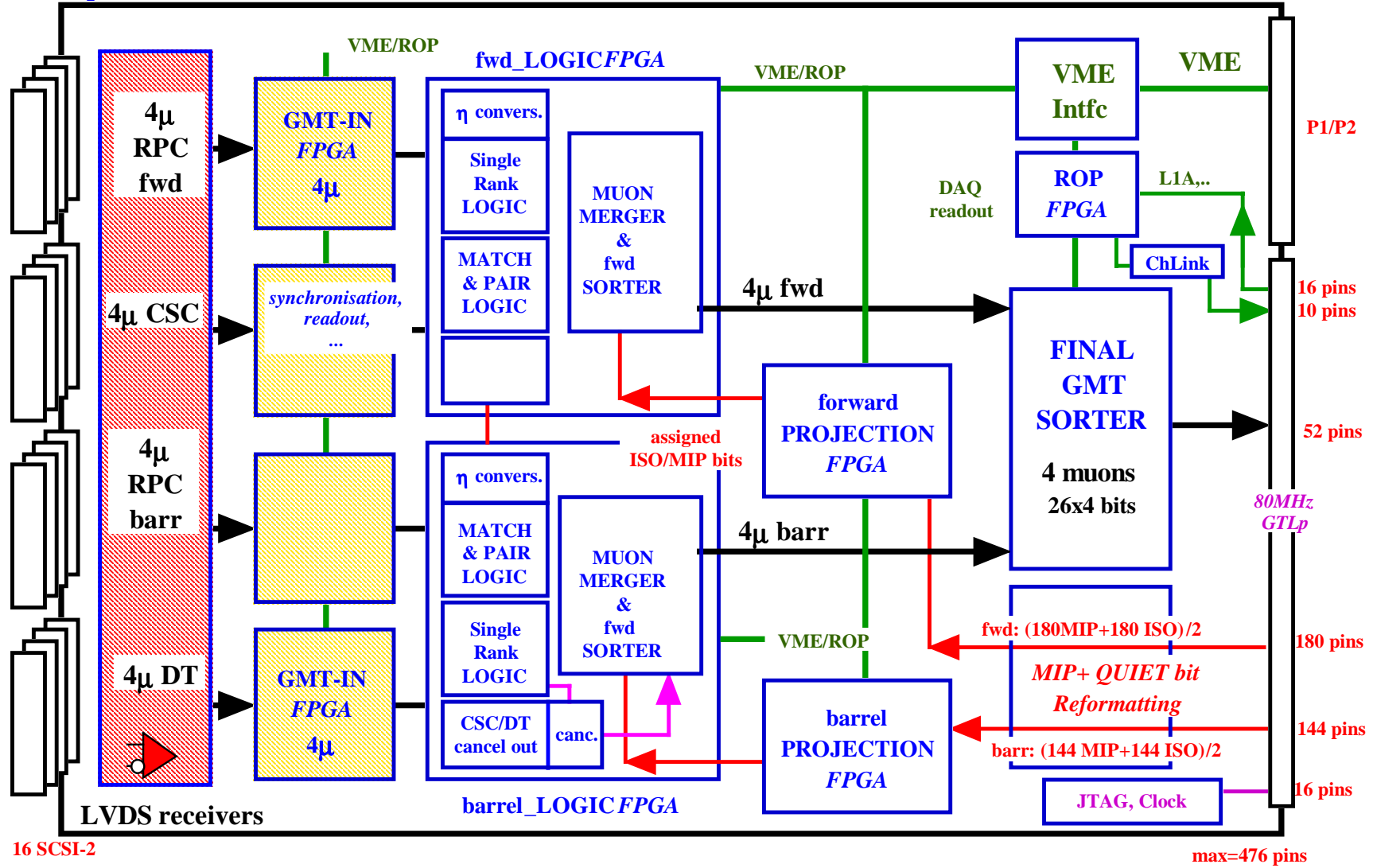


Global Trigger Crate

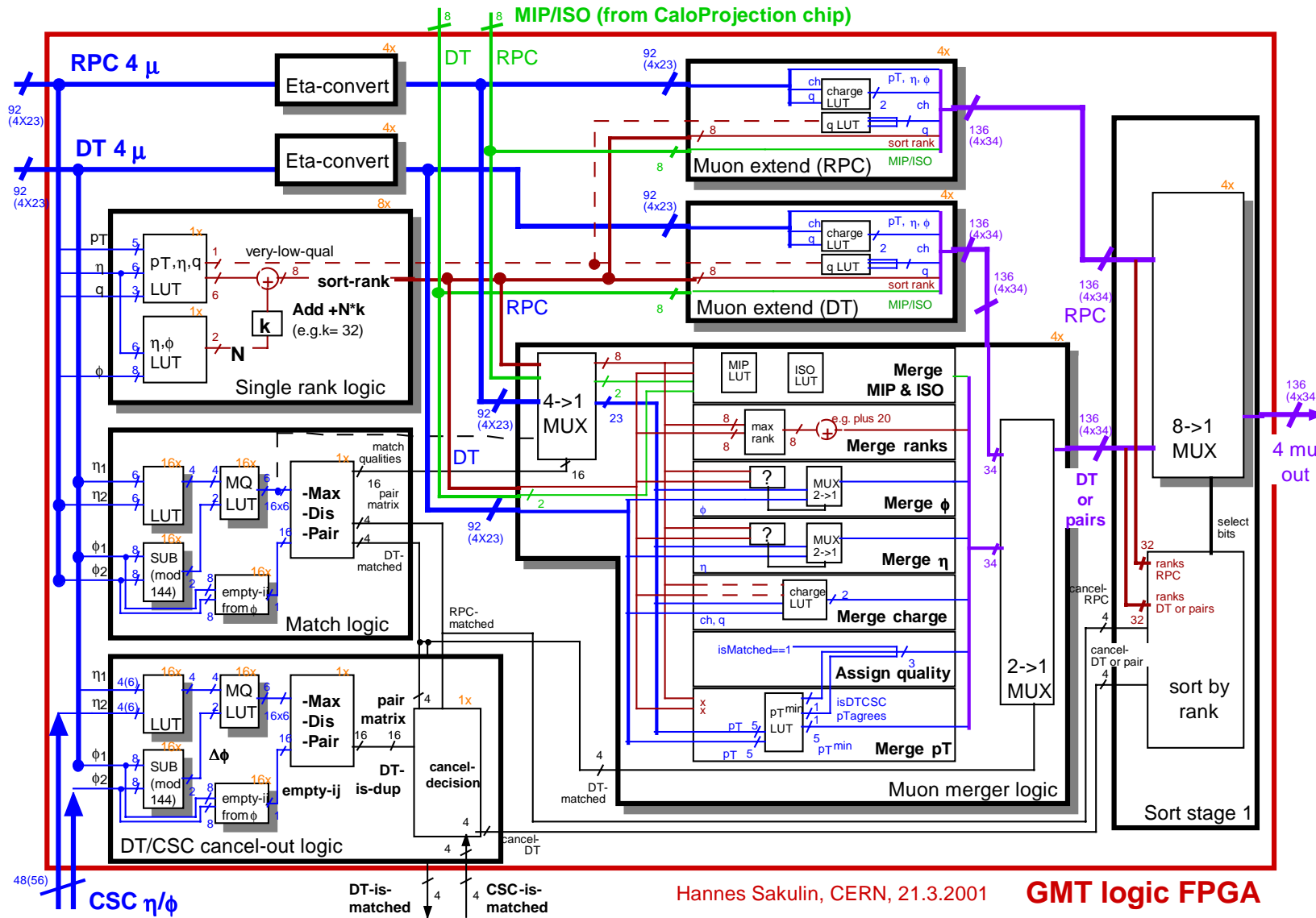


Single board Global Muon Trigger

Front panel



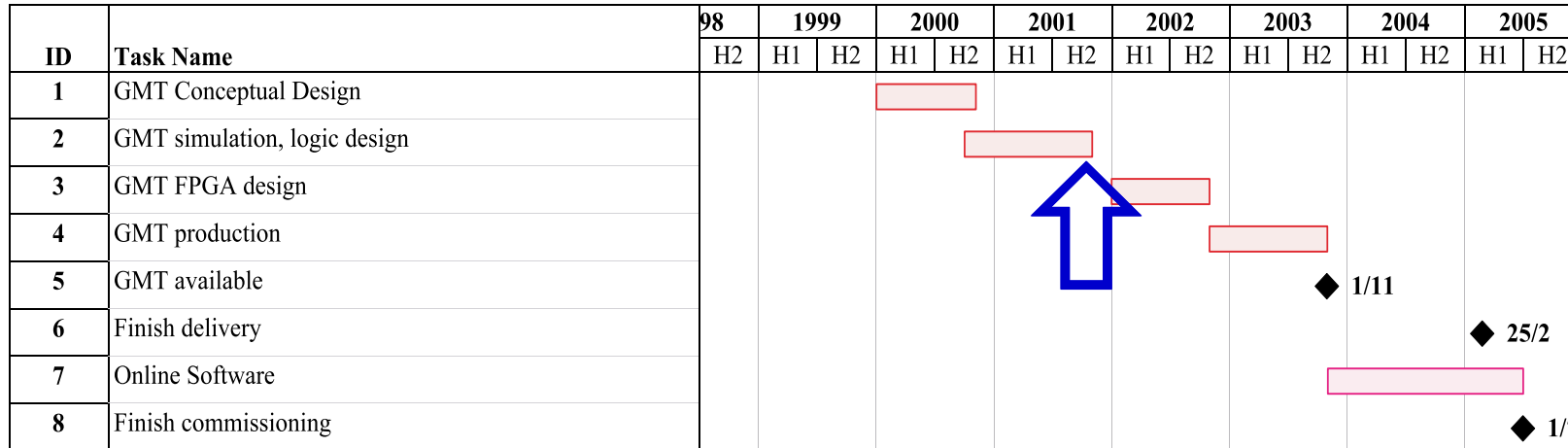
GMT Barrel Logic-FPGA



Hannes Sakulin, CERN, 21.3.2001

GMT logic FPGA

GMT Hardware schedule



- **Milestones / Plans:**

- 2001 Logic design, ORCA + VHDL Simulation
- **Dec 2001** Logic design finished
- 2002 VHDL Simulation, Design of FPGA chips
- **Dec 2002** FPGA design finished
- 2003 Production of VME 9U Boards
- 2004/05 Integration tests, production of spare boards

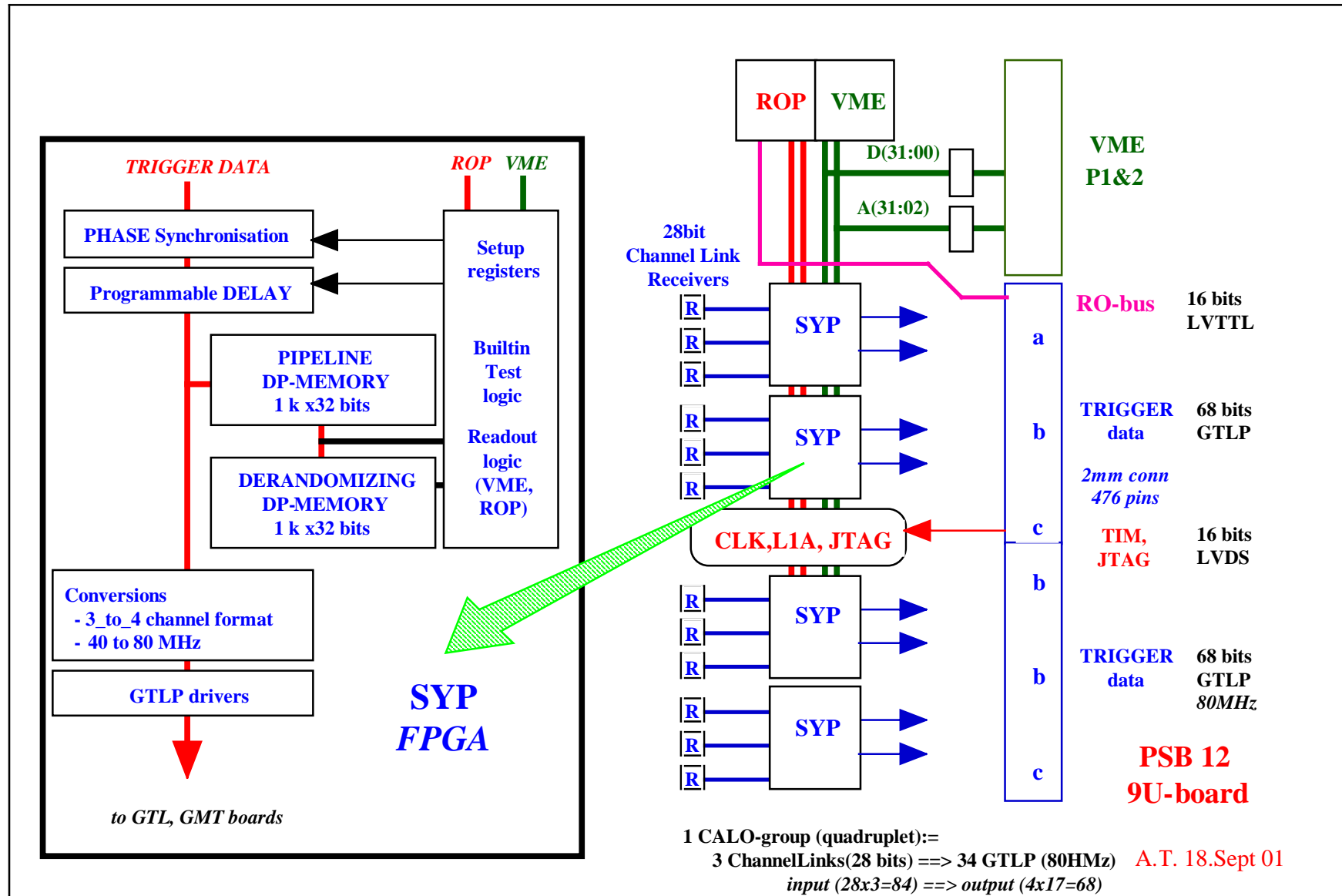
Progress towards GMT Milestones

- **Dec 2001:** **Logic design finished**
 - ✓ Progress in detailed logic design
 - Chip Models selected (mostly Virtex II), Interconnections defined
 - Design compacted (*external RAMs moved into big FPGAs*)
 - **Single board solution**
 - ✓ Improvement of functionality
 - DT/CSC cancel-out unit (improved performance in barrel/endcap overlap region)
 - ✓ in parallel:
 - ORCA Simulation extended and improved
 - Continuous studies to optimize GMT design parameters and performance
 - **CMS 2001/003** published: H. Sakulin, M. Fierro,
“**Studies of the Global Muon Trigger Performance**”
 - Detailed GMT design document in preparation
 - VHDL behavioral level simulation has started
- **Dec 2002:** **FPGA design finished**
 - ✓ FPGA models have been selected
 - Synthesis tools are being evaluated

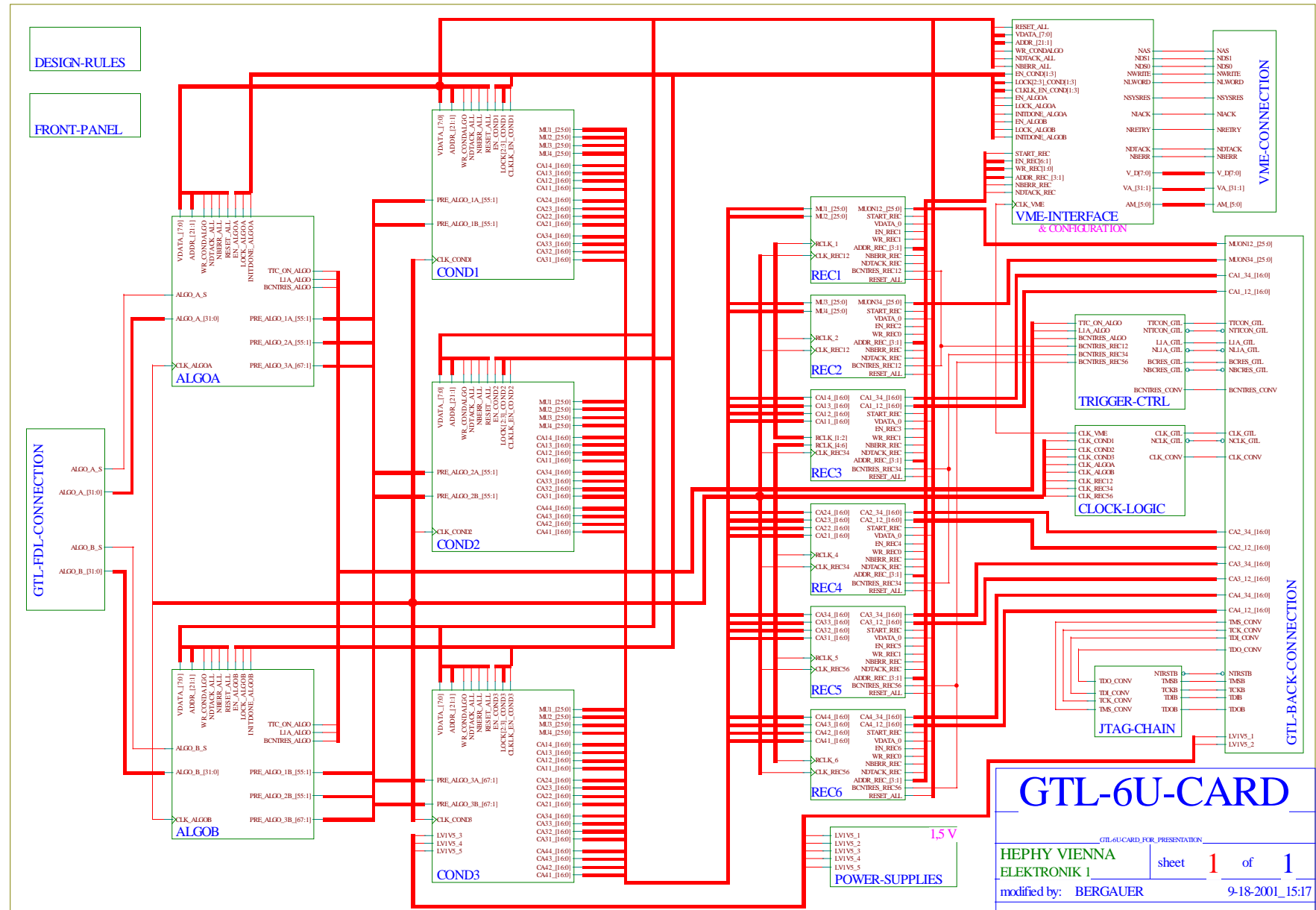
PSB 6 channel prototype



GMT, GT: Pipelined synchronizing buffer PSB board



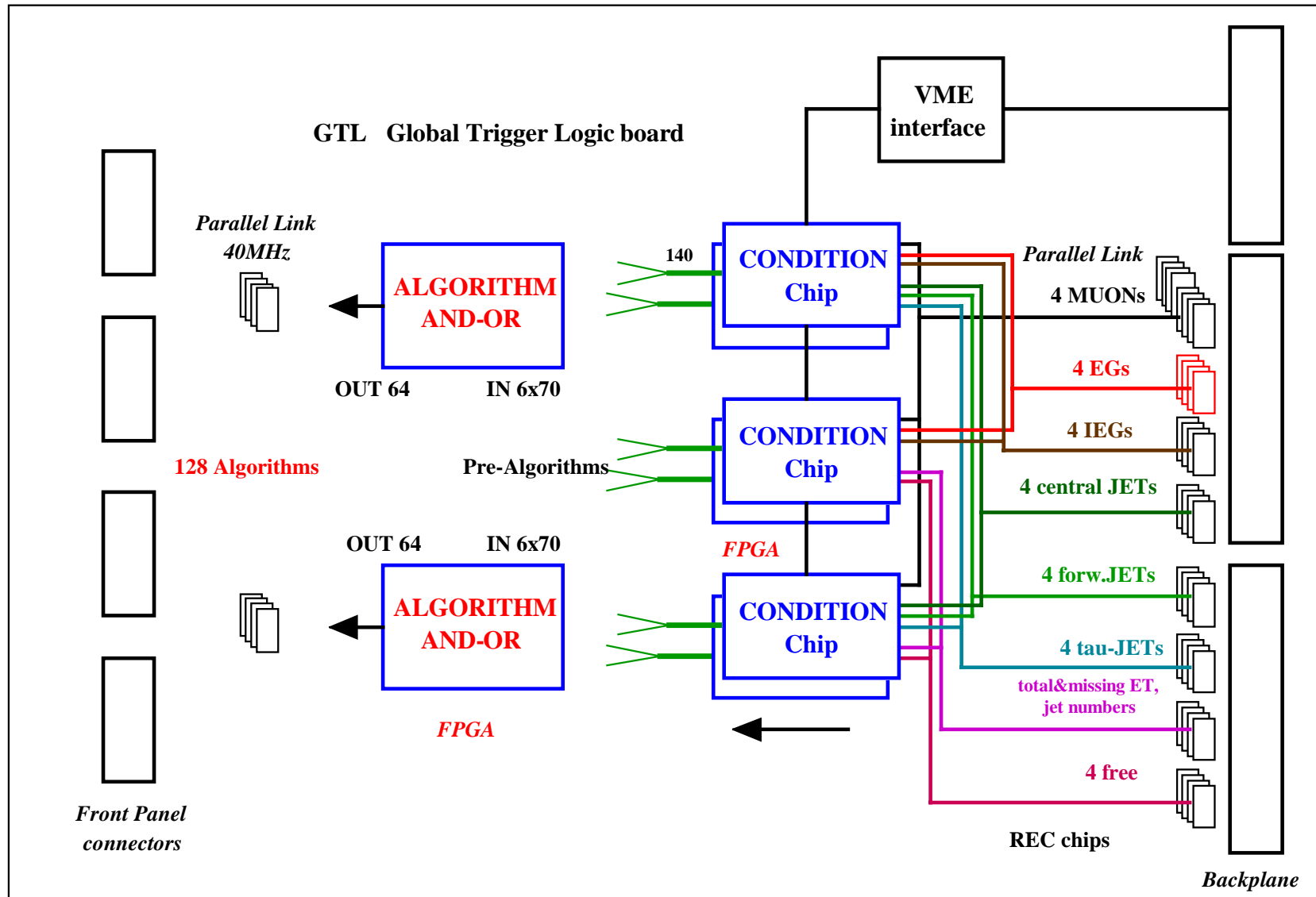
GTL prototype board schematic



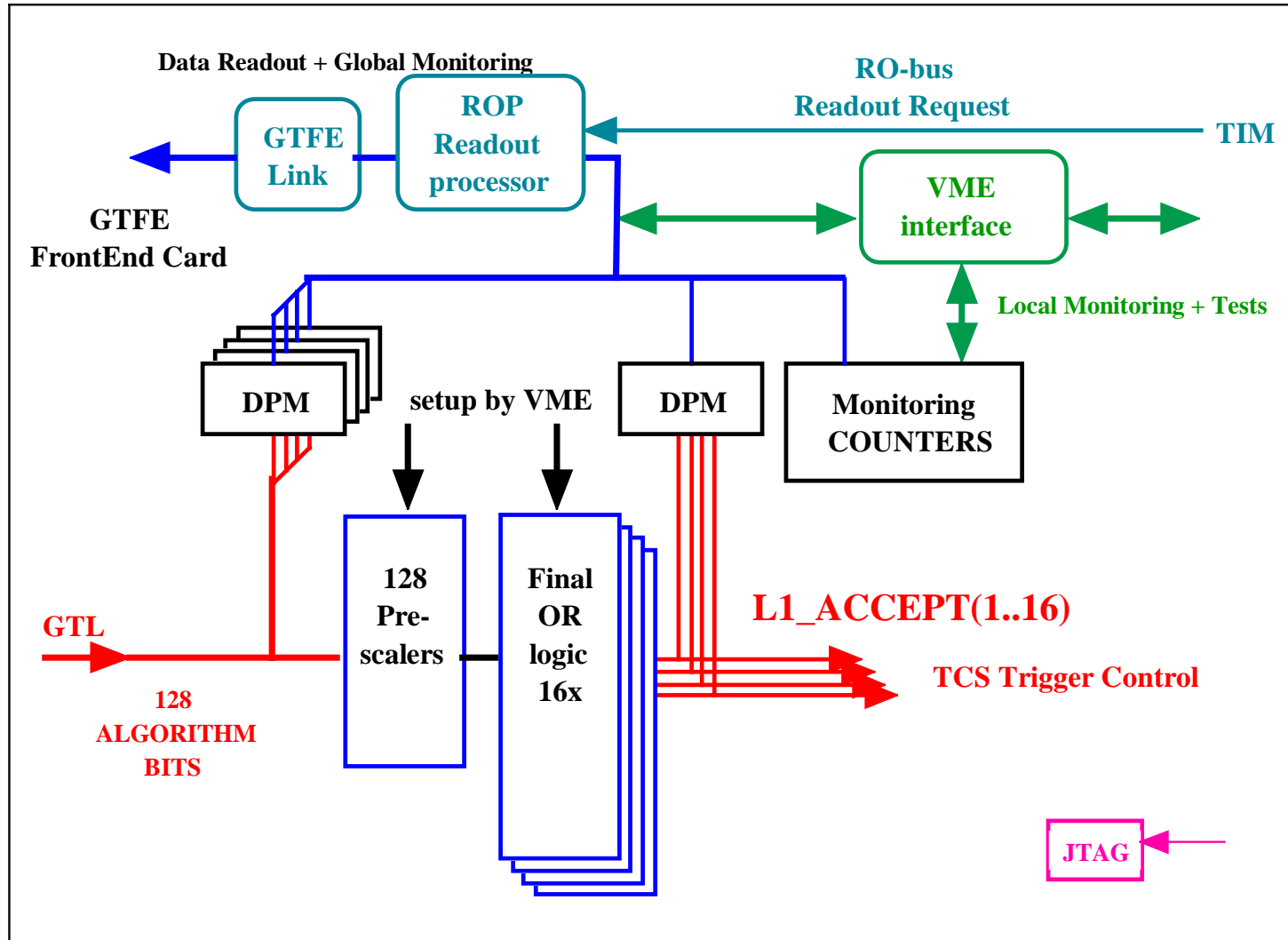
GTL-6U-CARD

GTL-6U-CARD_FOR_PRESENTATION

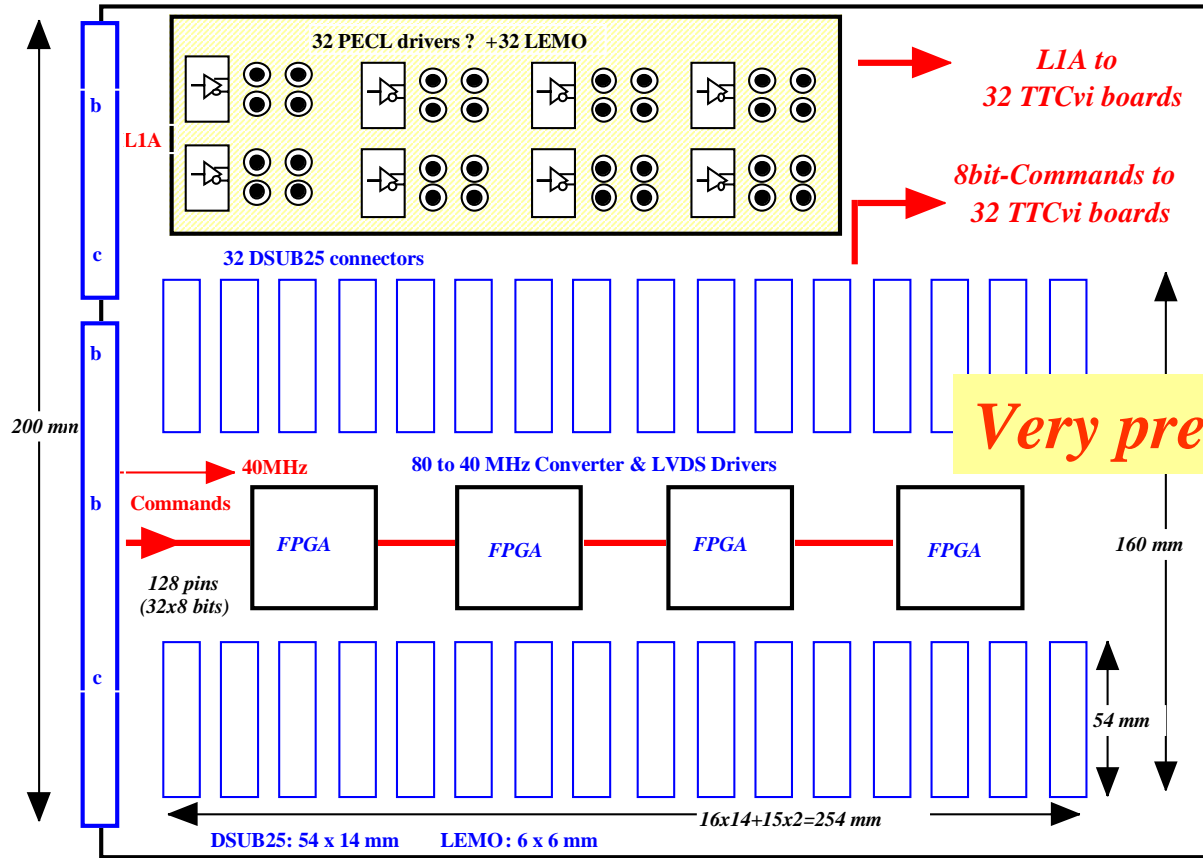
Global Trigger Logic board GTL9U



Final Decision Logic board FDL



L1A Driver board for a CMS-TTCvi



CMS-TTCvi:
12 (11) bit Command instead of B-Go, Trigger type.

Alternative1:
Send L1A as m.s. LVDS-bit also via the DSUB25 connectors.

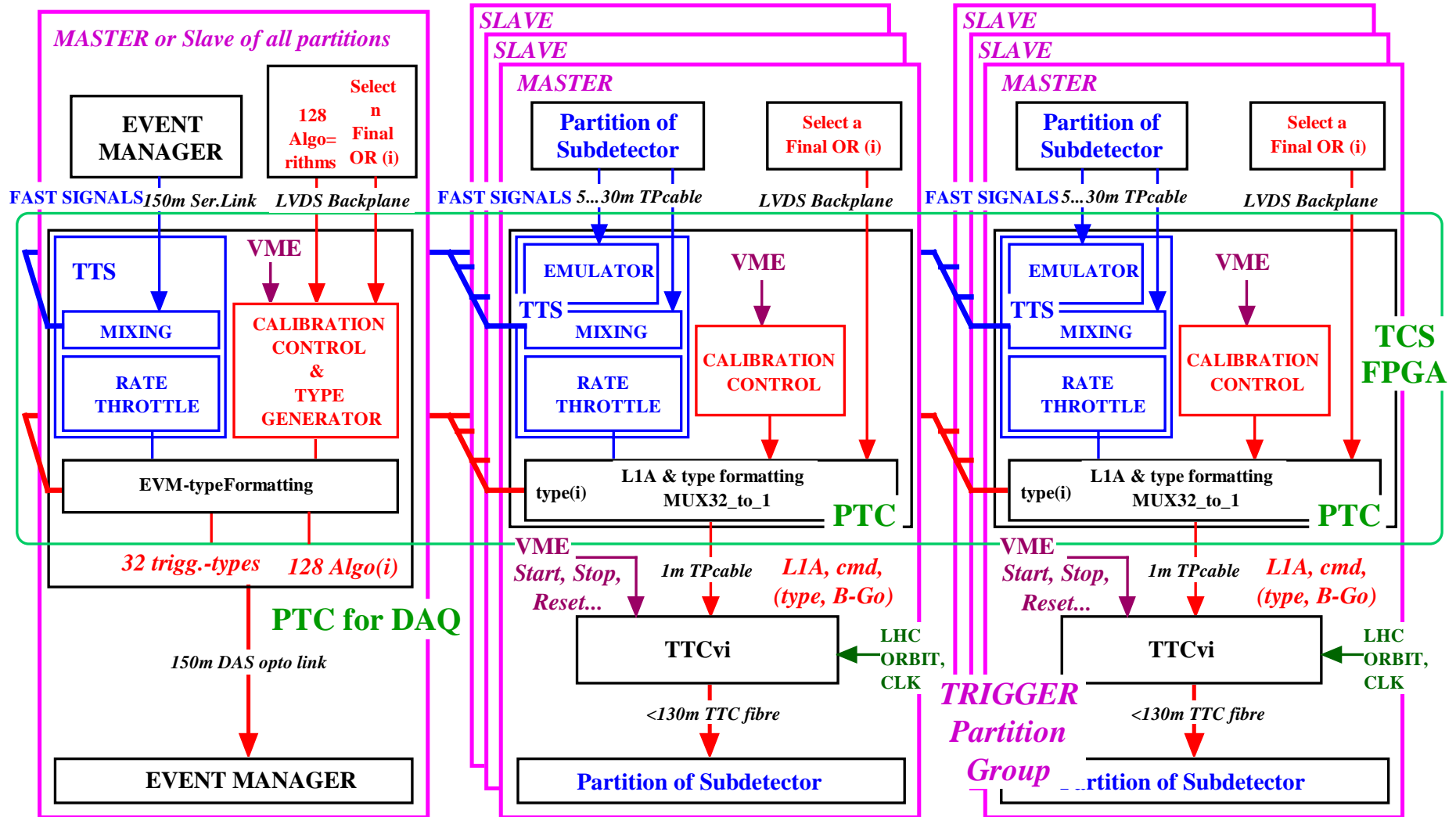
Very preliminary

Additional Requirements for the ATLAS-TTCvi:
32 ECL drivers (L1A),
96(128) NIM drivers (B-Go),
32 16-pin connectors (type),
128 LEMO connectors
====> require several output boards in an additional VME6Ucrate

CMS TTCvi:
(1 coax: L1A PECL low active)
DSUB25: 12 bits: Command + (L1A);
LVDS with 100 Ohm termination for a shielded TP cable

ATLAS TTCvi:
5 coax: L1A ECL low active, B-Go 0,1,2,3 NIM
2x8 pin : trigger type differential ECL with 120 Ohm termination for a 3M/3452-6600 (SCEM 09.55.03.316.4)

Trigger Partitions



TRIGGER PARTITION

= crates connected to 1 TTC tree
= component of subdetector

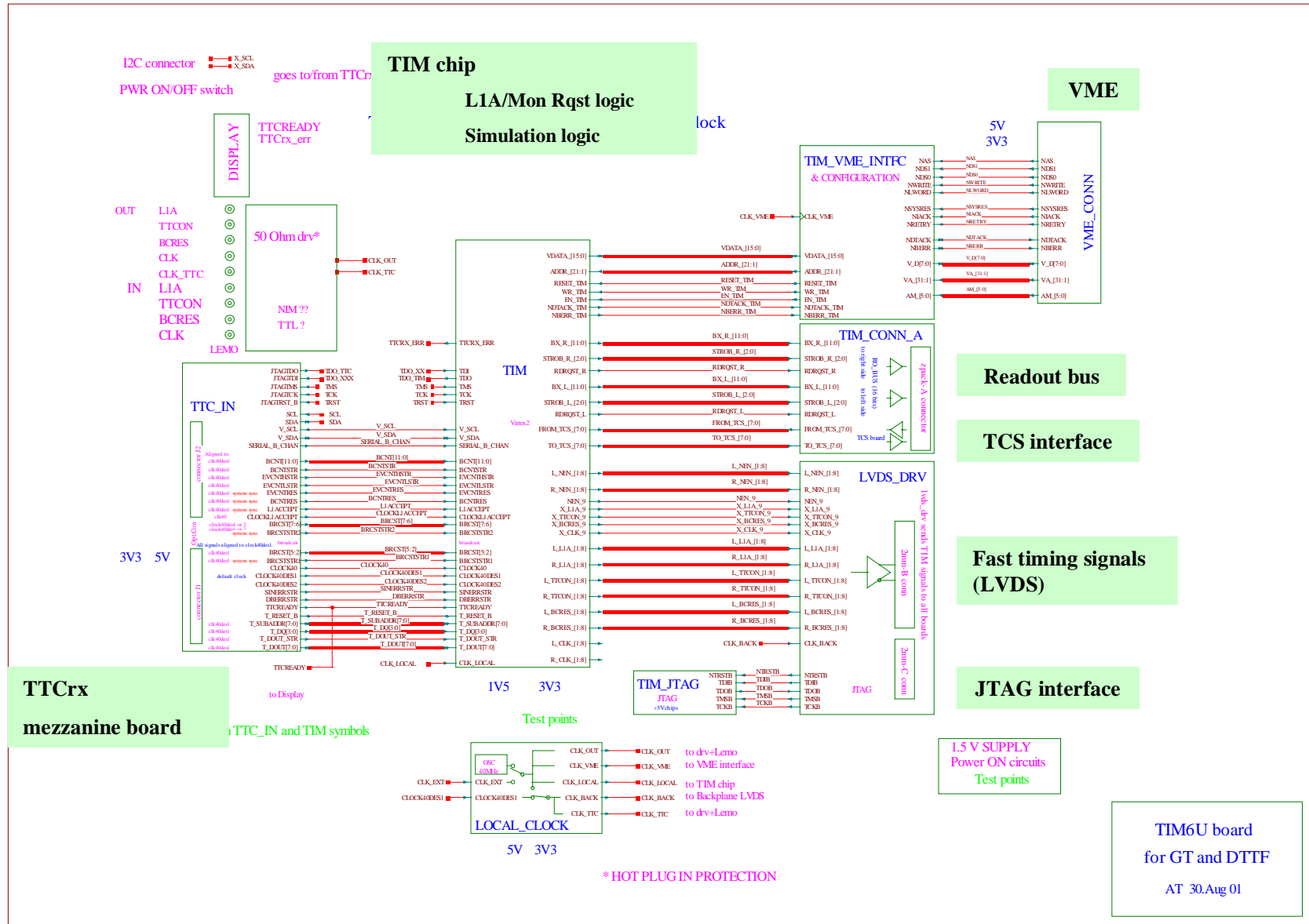
PTC = Partition Trigger Control

Group of Partitions

Example with 2 GROUPS

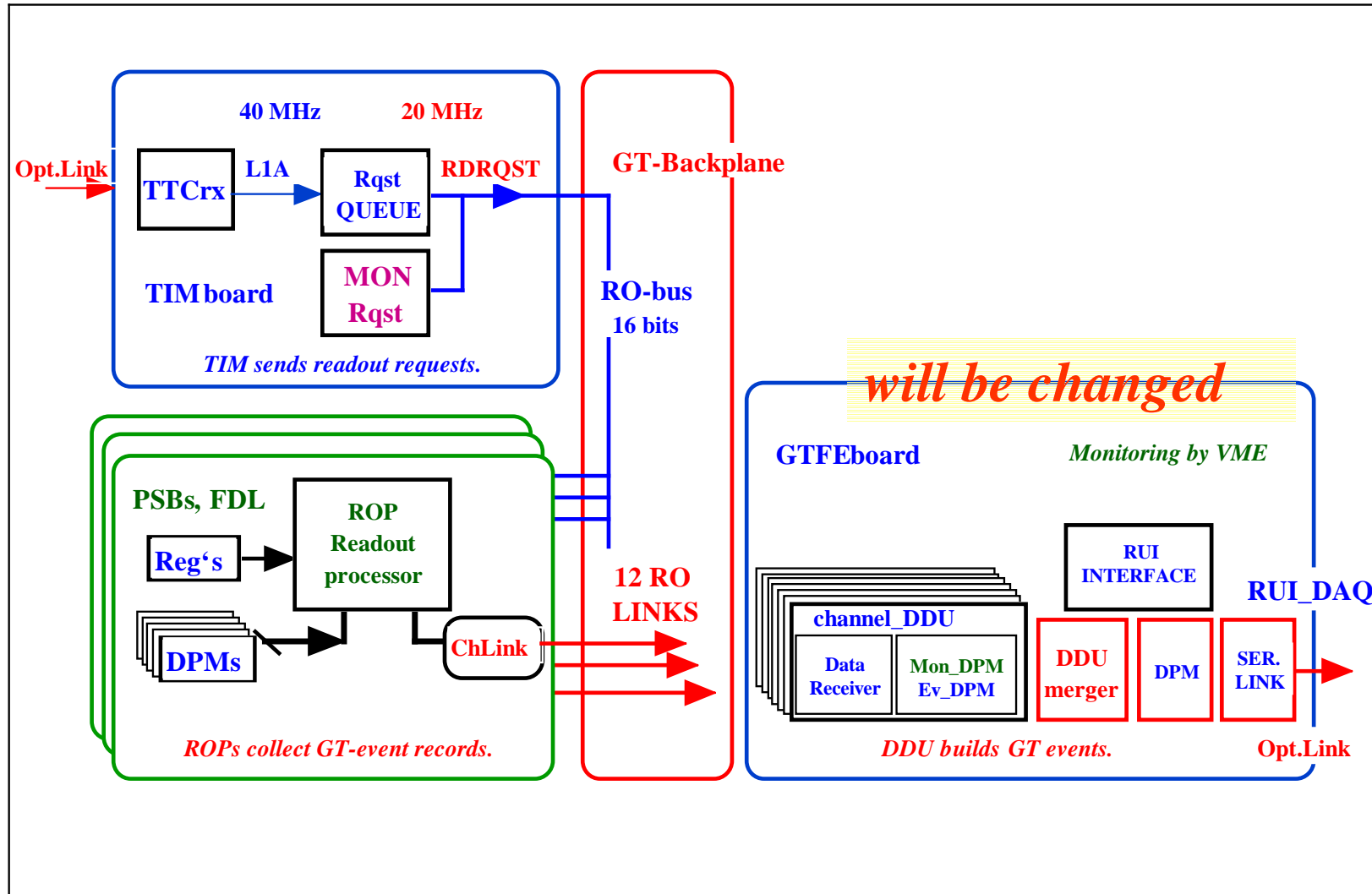
Trigger Control System

Schematic of TIMING board for GT, DTF



TIM6U board
for GT and DTF
AT 30.Aug 01

Timing and Readout Board



GMT/GT crate - Input / Output

- **1 TTC optical link**
- **Regional Muon Trigger data:** *GMT <==*
 - *Parallel LVDS data 40 MHz*
 - *68 pin SCSI-3 connectors,*
 - *Screened Round twisted pair cable (STP) : type to be defined*
- **Global Calorimeter Trigger data:** *GT <==*
 - *Channel Links 28 bits, 40 MHz rate (data are sent 2x with 80MHz)*
 - *SkewClear cable, Connectors to be defined*
- **Fast Signals: 32 cables** *TCS <==*
 - *Parallel LVDS data*
 - *5 pairs, cable and connectors to be defined (DSUB15 proposed)*
- **L1A and Commands to TTCvi: 32 cables** *==> TTCvi*
 - *to be defined...depends from CMS-TTCvi module*
- **2 S-Links to DAQ-PC (at bottom of rack)**
 - *S-link to DAQ-readout* *GT ==>*
 - *S-link to Event Manager* *TCS <==>*
 - *to be defined by DAQ group*

Global Trigger Hardware

- **Custom Backplane for VME 9U crate**
 - *80 MHz GTL-plus signals, Channel Links*
 - *2mm connectors, 160 pin VME connectors*
 - *Power Supplies: +5V, +3.3V, +2.5V, +1.8V*
- **PSB - Input board:**
 - *Channel Link receivers*
 - *Memories inside FPGA for Readout: 3-5 bx read by an L1A*
 - *Monitoring of all Input bits for every BX*
 - *Synchronisation checks for every BX*
- **GTL-Logic board:**
 - *FPGA loaded with different sets of algorithms: Physics-, Test-, Calibration Runs*
 - *Automatic Design Procedure*
- **FDL - Final Decision board**
 - *Monitoring of all Algorithm and L1A bits*
 - *Prescaling of all Algorithms*
 - *Trigger Mask*
 - *8 L1A's in parallel for Partition modes*

Global Trigger Hardware

- **TCS board:**
 - *Fast Signals: monitoring*
 - *Partitioning logic*
 - *Trigger Throttle logic and Calibration logic*
 - *S-Link to the Event Manager to transfer L1A-control data*
- **TIM board:**
 - *TTCrx chip or mezzanine board*
 - *Provides for all GT-boards Clock, BCReset and L1A signals, which are distributed as LVDS signals via the the backplane.*
 - *Control logic for L1A- Readout and Monitoring*
- **GTFE board**
 - *Interface to DAQ readout*
 - *S-Link to the DAQ to transfer trigger data*
 - *Monitoring Buffers...accessed by VME*
- **JTAG TEST**
 - *Access to boards via Backplane*
- **Control PC's: mounted at top of the rack**
 - *Linux, VME interface to 9U-GT crate and both standard 6U VME crates*

Global Trigger Hardware Status 09/01

| | status | MS =milestone |
|---|---------------------------|---------------|
| • Custom Backplane for VME 9U crate | | |
| – <i>6U Prototype: Channel Links,</i> | ...exists, necessary for | MS 3/02 |
| – <i>9U Backplane: 80MHz GTLp and Channel Links,</i> | ...design in progress | MS 10/02 |
| • PSB Input board (synchronisation, monitoring) | | |
| – <i>6 channel Prototype: Channel Link receivers</i> | ...exists , necessary for | MS 3/02 |
| – <i>12 channel board: memories inside FPGAs</i> | ... conceptual design | MS 7/04 |
| • GTL Logic board: | | |
| – <i>Conversion board for prototype</i> | ...layout done | MS 3/02 |
| – <i>GTL6U prototype: 20 channels</i> | ...layout in progress | MS 3/02 |
| • <i>4μ, 4ie/γ 4 cjets, 4 fjets, ETT,mET, 8 nr_of jets</i> | | |
| • <i>other quadruplets can be connected alternatively for tests</i> | | |
| – <i>GTL9U board: 32 channels</i> | ... conceptual design | MS 11/04 |
| • <i>4μ, 4ie/γ 4e/γ 4 cjets, 4 fjets, 4 tau_jets,ETT,mET, 8 nr_of jets, 4 free</i> | | |
| • TIM Timing board | ...schematic in progress | MS 3/02 |
| – 6U size, TTCrx, clock and L1A distribution, also used by DTF | | |
| • FDL-9U Final Decision board | ...design in progress | MS 3/02 |
| • TCS-9U Trigger Control board | ...design in progress | MS 7/02 |
| • GTFE-9U Readout board | ... conceptual design | MS 6/03 |